

**CLAIMS**

This claim list will replace all prior claim lists.

1. (Previously presented) A driver for driving a plasma display panel, wherein the plasma display panel includes a plurality of address electrodes, a plurality of X electrodes and a plurality of Y electrodes, said driver comprising:

an address driver;

an X driver; and

a Y driver,

wherein the plurality of X electrodes and the plurality of Y electrodes are arranged alternately next to each other to form XY electrode pairs and substantially perpendicular to the plurality of address electrodes,

wherein the XY electrode pairs are divided into a plurality of XY electrode pair groups,

at least one of the X driver and the Y driver comprises a plurality of driving circuits commonly connected to a reset circuit, each driving circuit corresponding to one of the plurality of XY electrode pair groups, and

in a mixed address-display period, a first XY electrode pair group is addressed and sustain-discharged by a first driving circuit before a second XY electrode pair group is addressed by a second driving circuit.

2. (Original) The driver of claim 1, wherein the plurality of driving circuits operate independently to perform an addressing operation and a display sustain discharge operation alternately and to apply a voltage for display-sustain discharge only to an XY electrode pair group that has already been addressed.

3. (Original) The driver of claim 1, wherein each of the plurality of driving circuits of the Y driver comprises:

a scan circuit that sequentially applies a scan pulse to the plurality of Y electrodes for addressing; and

a sustain circuit that simultaneously applies periodical display-sustain pulses of the alternating current voltage to the plurality of Y electrodes.

4. (Previously Presented) The driver of claim 3, wherein the scan circuit comprises:

a switching output circuit; and

a scan driving circuit.

5. (Previously Presented) The driver of claim 4, wherein the switching output circuit comprises:

an upper transistor;

a lower transistor; and

a common output line for the upper transistor and the lower transistor,

wherein the common output line is coupled to one of the plurality of Y electrodes.

6. (Previously presented) The driver of claim 5, wherein the scan circuit is coupled to an upper common power line of the upper transistor and to a lower common power line of the lower transistor to apply a scan voltage to one of the plurality of Y electrodes that is scanned during the mixed address-display period and to apply a scan bias voltage to one of the plurality of Y electrodes that is not scanned during the mixed address-display period.

7. (Original) The driver of claim 6, wherein an output of the sustain circuit is applied to

one of the upper common power line and the lower common power line via the scan driving circuit.

8. (Previously Presented) The driver of claim 3, wherein the reset circuit is arranged in the Y driver and performs a reset operation for having a state of charges in every display cell uniform.

9. (Original) The driver of claim 8, wherein the X driver comprises a single reset circuit that operates together with the reset circuit of the Y driver.

10. (Original) The driver of claim 8, wherein each of the plurality of driving circuits of the X driver comprises a sustain circuit which simultaneously applies periodical display-sustain pulses of the alternating current voltage to the X electrode lines.

11. (Original) The driver of claim 2, wherein each of the plurality of driving circuits of the Y driver drives Y electrodes of a corresponding XY electrode pair group, each of the plurality of driving circuits of the X driver drives X electrodes of a corresponding XY electrode pair group, wherein an XY electrode pair group including the plurality of Y electrodes driven by one among the plurality of driving circuits of the Y driver is not the same as an XY electrode pair group including the plurality of the X electrodes driven by one among the plurality of driving circuits of the X driver.

12. (Previously presented) A plasma display panel device, comprising:  
a plasma display panel;  
a video processor;

a logic controller;

an X driver that controls a plurality of X electrodes;

a Y driver that controls a plurality of Y electrodes; and

an address driver that controls a plurality of address electrodes,

wherein the plurality of Y electrodes and the plurality of X electrodes are arranged alternately next to each other to form XY electrode pairs,

wherein the XY electrode pairs are divided into a plurality of XY electrode pair groups, at least one of the X driver and the Y driver comprises a plurality of driving circuits commonly connected to a reset circuit, each driving circuit corresponding to one of the plurality of XY electrode pair groups, and

in a mixed address-display period, a first XY electrode pair group is addressed and sustain-discharged by a first driving circuit before a second XY electrode pair group is addressed by a second driving circuit.